

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	PFET-BASED ESD PROTECTION STRATEGY FOR IMPROVED EXTERNAL LATCH-UP ROBUSTNESS																																																																																																																																																																
<p>Application Number :</p> <p>Confirmation Number:</p> <p>First Named Applicant: Kiran Chatty</p> <p>Attorney Docket Number: BUR920030045US1</p> <p>Art Unit:</p> <p>Examiner:</p> <p>Search string: (5140401 or 5208719 or 5287241 or 5304839 or 5440162 or 5477413 or 5479039 or 5637900 or 5644459 or 5719733 or 5745323 or 5783850 or 5869873 or 5872378 or 5907464 or 5939753 or 5946175 or 5991134 or 5998247 or 6033949 or 6040603 or 6046087 or 6157065 or 6181214 or 6215156 or 6232206 or 6256184 or 6309940 or 6337787 or 6411480 or 6417541 or 6476449 or 6563176 or 6566715 or 6566717 or 6566911 or 20010010954 or 20020105766 or 20020115250 or 20020118499 or 20020153564 or 20020154463 or 20020195663 or 20020195665),pn</p>																																																																																																																																																																	
<p>US Patent Documents</p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>init</th> <th>Cite.No.</th> <th>Patent No.</th> <th>Date</th> <th>Patentee</th> <th>Kind</th> <th>Class</th> <th>Subclass</th> </tr> </thead> <tbody> <tr><td>0N</td><td>1</td><td>5140401</td><td>1992-08-18</td><td>Ker et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>2</td><td>5208719</td><td>1993-05-04</td><td>Wei</td><td></td><td></td><td></td></tr> <tr><td></td><td>3</td><td>5287241</td><td>1994-02-15</td><td>Puar</td><td></td><td></td><td></td></tr> <tr><td></td><td>4</td><td>5304839</td><td>1994-04-19</td><td>Chen et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>5</td><td>5440162</td><td>1995-08-08</td><td>Worley et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>6</td><td>5477413</td><td>1995-12-19</td><td>Watt</td><td></td><td></td><td></td></tr> <tr><td></td><td>7</td><td>5479039</td><td>1995-12-26</td><td>Lien</td><td></td><td></td><td></td></tr> <tr><td></td><td>8</td><td>5637900</td><td>1997-06-10</td><td>Ker et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>9</td><td>5644459</td><td>1997-06-01</td><td>Lien</td><td></td><td></td><td></td></tr> <tr><td></td><td>10</td><td>5719733</td><td>1998-02-17</td><td>Wei et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>11</td><td>5745323</td><td>1998-04-27</td><td>English et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>12</td><td>5783850</td><td>1998-06-21</td><td>Liau et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>13</td><td>5869873</td><td>1999-02-19</td><td>Yu</td><td></td><td></td><td></td></tr> <tr><td></td><td>14</td><td>5872378</td><td>1999-02-16</td><td>Rose et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>15</td><td>5907464</td><td>1999-05-25</td><td>Maloney et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>16</td><td>5939753</td><td>1999-08-17</td><td>Ma et al.</td><td></td><td></td><td></td></tr> <tr><td></td><td>17</td><td>5946175</td><td>1999-08-31</td><td>Yu</td><td></td><td></td><td></td></tr> <tr><td></td><td>18</td><td>5991134</td><td>1999-11-23</td><td>Tan et al.</td><td></td><td></td><td></td></tr> <tr><td>0P</td><td>19</td><td>5998247</td><td>1999-12-07</td><td>Wu</td><td></td><td></td><td></td></tr> </tbody> </table>		init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	0N	1	5140401	1992-08-18	Ker et al.					2	5208719	1993-05-04	Wei					3	5287241	1994-02-15	Puar					4	5304839	1994-04-19	Chen et al.					5	5440162	1995-08-08	Worley et al.					6	5477413	1995-12-19	Watt					7	5479039	1995-12-26	Lien					8	5637900	1997-06-10	Ker et al.					9	5644459	1997-06-01	Lien					10	5719733	1998-02-17	Wei et al.					11	5745323	1998-04-27	English et al.					12	5783850	1998-06-21	Liau et al.					13	5869873	1999-02-19	Yu					14	5872378	1999-02-16	Rose et al.					15	5907464	1999-05-25	Maloney et al.					16	5939753	1999-08-17	Ma et al.					17	5946175	1999-08-31	Yu					18	5991134	1999-11-23	Tan et al.				0P	19	5998247	1999-12-07	Wu			
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Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/604,922
		Filing Date	August 27, 2003
		First Named Inventor	Kiran V. CHATTY
		Art Unit	To Be Assigned
		Examiner Name	To Be Assigned
Sheet	1	of	1
		Attorney Docket Number	BUR920030045US1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Already filed electronically on Sep. 4, 2003.

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁵
		Country Code ² -Number ³ -Kind Code ⁴ (if known)				
ON	✓	EP 1045444 A1	10-18-2000	Chen		
ON	✓	JP 10-50494	02-20-1998	Knight et al.		
ON	✓	JP 10-294445	11-04-1998	Szafranski et al.		

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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
DN	✓	Ming-Dou KER, "ESD Protection for CMOS Output Buffer by Using Modified LVTSCR Devices with High Trigger Current," IEEE Journal of Solid State Circuits, Vol. 32, No. 8, Aug. 1997, pp. 1293-96.			
	✓	Ming-Dou KER and Hun-Hsien CHANG, "How to Safely Apply the LVTSCR for CMOS Whole-Chip ESD Protection without being Accidentally Triggered On," 1998 EOS/ESD Symposium, pp. 72-85.			
	✓	Jeremy C. SMITH, "An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Condition During EOS/ESD Events," 1999 EOS/ESD Symposium, pp. 62-69.			
	✓	Teruo SUZUKI et al., "A Study of Fully Silicided 0.18um CMOS ESD Protection Devices," 1999 EOS/ESD Symposium, pp. 78-87.			
DN	✓	Gianluca BOSELLI et al., "Efficient pnp Characteristics of pMOS Transistors in Sub-0.13um ESD Protection Circuits," 2002 EOS/ESD Symposium, pp. 257-66.			

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Examiner Signature	<i>ON</i>	Date Considered	11/17/03
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ON	20	6033949	2000-03-07	Baker et al.			
	21	6040603	2000-03-21	Yang			
	22	6046087	2000-04-04	Lin et al.			
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init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
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	2	20020105766	2002-08-08	Lin et al.			
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	7	20020195663	2002-12-26	Ramsbey et al.			
ON	8	20020195665	2002-12-26	Jun et al.			

Signature

Examiner Name	Date
ON	11/17/05